CLAIMS

WHAT IS CLAIMED IS:

1. A method of masking a ringing in a DQS signal having a finite number of pulses in a memory device including a DDR SDRAM, the method comprising the steps of:

(a) receiving a DQS signal by a DQS buffer for use within the DDR SDRAM and outputting to a DQS latch;

(b) receiving data having a plurality of data bursts by a data input buffer and outputting to a data input latch;

(c) generating a first signal in synchronization with a rising edge of a first pulse of the DQS signal and a second signal in synchronization with a falling edge of the first pulse of the DQS signal,

wherein the first and second signals are generated by the DQS latch and outputted to the data input latch;

(d) storing in the data input latch a first data burst outputted from the data input buffer in synchronization with a rising edge of the first signal;

(e) storing in the data input latch a second data out outputted from the data input buffer in synchronization with a rising edge of the second signal;

(f) transferring the first and second data stored in the data input latch to a data input/output detection amplifier (Din IOSA) in synchronization with one of data input strobe pulses; and

(g) determining a point in time at which the burst length of the data ends and controlling the operations of the DQS buffer to enable or disable the generation of the first and second signals after determining the point in time at which the burst length of the data ends.

2. The method of claim 1, wherein the step (g) comprises the steps of:

(g-1) generating a first pulse signal when a write command is issued;

(g-2) generating at least four write burst signals comprising a first to a fourth write burst signals according to the first pulse signal and the burst length, the first burst signal being enabled during the burst length;

(g-3) generating a second pulse signal in synchronization with a clock signal of the DDR SDRAM while the first write burst signal is enabled;

(g-4) generating a third pulse signal for disabling the first write burst signal according to the burst

length by a combination of the first and second pulse signals;

(g-5) generating a fourth pulse signal for disabling the operation of the DQS buffer in synchronization with the second signal of step (c) after the first write burst signal is disabled; and

(g-6) disabling the fourth pulse signal using the second to fourth write burst signals to normally operate the DQS buffer.

3. The method as claimed in claim 2,

wherein the first write burst signal is enabled during the burst length by a first pulse signal generated in response to the write command,

wherein the second write burst signal is a signal obtained by delaying the first write burst signal by one half period of the clock signal,

wherein the third write burst signal is a signal obtained by delaying the second write burst signal by one half period of the clock signal, and

wherein the fourth write burst signal is a signal obtained by delaying the third write burst signal by one half period of the clock signal.

4. A device for masking ringing in a DQS signal in a memory

device including a DDR SDRAM, comprising:

a DQS buffer for receiving a DQS signal;

a DQS latch for storing the DQS signal outputted from the DQS buffer;

a data buffer for receiving data having a plurality of data bursts;

a data latch for storing the data transferred from the data buffer; and

a data input/output detection amplifier for receiving the data stored in the data latch and transferring the received data to global input/output lines; and

means for controlling the operations of the DQS buffer based on a determined point in time, wherein the determined pointed in time is the point in time at which the burst length ends after receiving a write command.

5. The device as claimed in claim 4, wherein the means for controlling an operation of the DQS buffer comprises:

a write command decoder for generating a first pulse signal when the write command is issued;

a write burst generator for generating a first to a fourth write burst signal according to the first pulse signal and the burst length, the first write burst

signal being enabled during the burst length,

an internal write generator for generating a second pulse signal in synchronization with a clock signal of the DDR SDRAM while the first write burst signal is enabled,

a burst length counter for generating a third pulse signal, which disables the first write burst signal according to the burst length, by a combination of the first and second pulse signals, and

a DQS controller for generating a fourth pulse signal, which controls the operation of the DQS buffer, in synchronization with a falling edge of the DQS signal after the first write burst signal is disabled.

6. The device as claimed in claim 5, wherein the first write burst signal is enabled by the first pulse signal during the burst length, the second write burst signal is a signal obtained by delaying the first write burst signal by one half period of the clock signal, the third write burst signal is a signal obtained by delaying the second write burst signal by one half period of the clock signal, the fourth write burst signal is a signal obtained by delaying the third write burst signal by one half period of the clock signal, and the fourth pulse signal is disabled by the second

to fourth write burst signals and the DQS buffer normally operates when the fourth pulse signal is disabled.

7. The device as claimed in claim 5, wherein the write burst generator receives the second pulse signal and counts the third pulse signal.

8. A device for masking a ringing in a DQS signal in a memory device including a DDR SDRAM, comprising:

means for performing a write operation; and

means for generating a control signal which determines an end point in time of a burst length to disable the operation of the DQS buffer based on the determined point in the time and normally recovers the operation of the DQS buffer after the elapse of a predetermined time, when a write command is issued,

wherein the means for performing a write operation comprises:

a DQS buffer for receiving a DQS signal;

a DQS latch for storing the DQS signal outputted from the DQS buffer;

a data buffer for receiving data;

a data latch for storing the data transferred from the data buffer; and

a data input/output detection amplifier for receiving the data stored in the data latch and transferring the received data to global input/output lines.

9. A method of masking a ringing in a DQS signal in a memory device including a DDR SDRAM having a DQS buffer for receiving and buffering the DQS signal for use within the DDR SDRAM, wherein the DQS signal is utilized for accessing data having a burst length, the method comprising the steps of:

(a) determining a point in time at which the burst length ends;

(b) disabling the DQS buffer in response to a first burst signal enabled in a burst mode operation; and

(c) enabling the DQS buffer in response to a second burst signal enabled in a burst mode operation.

10. In a memory device including a DDR SDRAM that operates at a double data rate by accessing the bursts of data (DQ) having a burst length (n) in accordance with the rising and falling edges of each pulse of a DQS signal, a device for masking a ringing that corrupts the integrity of the DQS signal causing write failures, the device comprising:

a DQS buffer (330) for generating a first access

signal (dsrt2) substantially in synchronization with the rising edge of each DQS pulse generated in presence of the data burst (DQ) and for generating a second access signal (dsft2) substantially in synchronization with the falling edge of each DQS pulse generated in presence of the data burst (DQ),

wherein the first access signal (dsrt2) includes a finite number of pulses based on the total number of rising edges of the DQS signal,

wherein the second access signal (dsft2) includes a finite number of pulses based on the total number of falling edges of the DQS signal, and

wherein two consecutive data bursts are accessed together for a write operation for each pair of the consecutive first and second access signals (dsrt2, dsft2); and

means (300, 310, 320, 340, 350) for disabling the DQS buffer for a mask time (dsb) after accessing all data bursts,

wherein the mask time (dsb) is calculated based on at least the second access signal (dsft2) and the data burst length (n),

and

further wherein the calculated mask time sufficiently includes the duration of time in which a ringing is present in the DQS signal, so that the disablement of the DQS buffer (330) during the mask time (dsb) prevents a write failure caused by the corrupted DQS signal with the ringing.

11. The device of claim 10, wherein the mask time (dsb) begins when the last pulse of the second access signal (dsft2) is detected.

12. The device of claim 11, wherein the mask time (dsb) ends after a predetermined delay from the detection of the second access signal (dsft2), wherein the predetermined delay is proportional to the number of data bursts (n) and the period of one clock cycle.

13. The device of claim 12, wherein the predetermined delay substantially equals the time of one half period of one clock cycle multiplied by the number of data bursts (n).

14. The device of claim 10, wherein the mask time (dsb)

begins substantially at the falling edge of the last pulse of the DQS signal.

15. The device of claim 14, wherein the mask time (dsb) ends after a predetermined delay from the detection of the second access signal (dsft2), wherein the predetermined delay is proportional to the number of data bursts (n) and the period of one clock cycle.

16. The device of claim 15, wherein the predetermined delay substantially equals the time of one half period of one clock cycle multiplied by the number of data bursts (n).

17. The device of Claim 10, wherein means for disabling the DQS buffer comprises:

a write command decoder (300) for receiving the write command and generating a write command pulse (wtp6) based on the write command;

means (310, 320, 350) for generating a number of data length signals (wt_burst0,1,2,3...n), after receiving the write command pulse (wtp6) from the write command decoder,

wherein the number of generated data length signals (n) equals the number of data

bursts (n);

wherein the duration in which each data length signal (wt_burst) is enabled equals the total length of the data bursts;

wherein a first data length signal (wt_burst0) is enabled by the write command pulse (wtp6); and

wherein each of the subsequent data length signals (wt_burst1,2,3... or n) is substantially identical to the previous one of the data length signals (wt_burst0,1,2,3... or n-1) but delayed by one half clock period (tclk); and

a DQS controller for receiving the data length signals (wt_burst0,1,2,3...n) and the second access signal (dsft2) and generating a mask signal (dsb) to the DQS buffer,

wherein the mask signal (dsb) includes a duration of the masking time in which the DQS buffer is to be disabled,

wherein the beginning of the masking time is substantially synchronized with the second access signal (dsft2), and

further wherein the end of the masking

time is substantially synchronized with the falling edge of the last data length signal (wt_burstn).

18. The device of claim 17, wherein the mask time (dsb) begins when the last pulse of the second access signal (dsft2) is detected.

19. The device of claim 18, wherein the mask time (dsb) ends after a predetermined delay from the detection of the second access signal (dsft2), wherein the predetermined delay is proportional to the number of data bursts (n) and the period of one clock cycle.

20. The device of claim 19, wherein the predetermined delay substantially equals the time of one half period of one clock cycle multiplied by the number of data bursts (n).

21. The device of claim 17, wherein the mask time (dsb) begins substantially at the falling edge of the last pulse of the DQS signal.

22. The device of claim 18, wherein the mask time (dsb) ends after a predetermined delay from the detection of the second

access signal (dsft2), wherein the predetermined delay is proportional to the number of data bursts (n) and the period of one clock cycle.

23. The device of claim 19, wherein the predetermined delay substantially equals the time of one half period of one clock cycle multiplied by the number of data bursts (n).

24. In a memory device including a DDR SDRAM that operates at a double data rate by accessing the bursts of data (DQ) having a burst length (n) in accordance with the rising and falling edges of each pulse of a DQS signal, a method of masking a ringing that corrupts the integrity of the DQS signal causing write failures, the method comprising the steps of:

generating a first access signal (dsrt2) substantially in synchronization with the rising edge of each DQS pulse generated in presence of the data burst (DQ);

generating a second access signal (dsft2) substantially in synchronization with the falling edge of each DQS pulse generated in presence of the data burst (DQ),

wherein the first access signal (dsrt2)

includes a finite number of pulses based on the total number of rising edges of the DQS signal,

wherein the second access signal (dsft2) includes a finite number of pulses based on the total number of falling edges of the DQS signal, and

wherein two consecutive data bursts are accessed together for a write operation for each pair of the consecutive first and second access signals (dsrt2, dsft2); and

after accessing all data bursts, generating no additional first and second access signals (dsrt2, dsft2) for a calculated mask time (dsb),

wherein the mask time (dsb) is calculated based on at least the last pulse of the already generated second access signal (dsft2) and the data burst length (n), and

further wherein the calculated mask time sufficiently includes the duration of time in which a ringing is present in the DQS signal, so that by not generating the additional first and second access signals (dsft2, dsrt2) during the mask time (dsb), a write failure

caused by the corrupted DQS signal is prevented.

25. The method of claim 24, wherein the mask time (dsb) begins when the last pulse of the second access signal (dsft2) is detected.

26. The method of claim 25, wherein the mask time (dsb) ends after a predetermined delay from the detection of the second access signal (dsft2), wherein the predetermined delay is proportional to the number of data bursts (n) and the period of one clock cycle.

27. The method of claim 26, wherein the predetermined delay substantially equals the time of one half period of one clock cycle multiplied by the number of data bursts (n).

28. The method of claim 24, wherein the mask time (dsb) begins substantially at the falling edge of the last pulse of the DQS signal.

29. The method of claim 28, wherein the mask time (dsb) ends after a predetermined delay from the detection of the second access signal (dsft2), wherein the predetermined delay is

proportional to the number of data bursts (n) and the period of one clock cycle.

30. The method of claim 29, wherein the predetermined delay substantially equals the time of one half period of one clock cycle multiplied by the number of data bursts (n).

31. The method of claim 24, wherein the method of generating no additional first and second access signals (dsrt2, dsft2) for a calculated mask time (dsb) after accessing all data bursts further comprises steps of:

receiving a write command;

generating a write command pulse (wtp6) based on the write command;

generating a number of data length signals (wt_burst0,1,2,3...n-1), after receiving the write command pulse (wtp6) from the write command decoder,

wherein the number of generated data length signals (n) equals the number of data bursts (n);

wherein the duration in which each data length signal (wt_burst) is enabled equals the total length of the data bursts;

wherein a first data length signal

(wt_burst0) is enabled by the write command pulse (wtp6); and

wherein each of the subsequent data length signals (wt_burst1,2,3... or n-1) is substantially identical to the previous one of the data length signals (wt_burst0,1,2,3... or n-2) but delayed by a one half clock period (tclk); and

generating a mask signal (dsb) based on the data length signals (wt_burst0,1,2,3...n) and the second access signal (dsft2),

wherein the beginning of the masking time is substantially synchronized with the last pulse of the second access signal (dsft2), and

further wherein the end of the masking time is substantially synchronized with the falling edge of the last data length signal (wt_burstn-1).